REMARKS

Please refer to Fig.3 and Fig.4. The frequency divider 30 shown in Fig.3 comprises two dividing circuits 34 and 36, each of which comprises a front set circuit, a middle set circuit, and a rear set circuit. The middle set circuit 44 of the dividing circuit 34 comprises a rising-edge-triggered clock generator 66 and an output end A for outputting divided clocks with a frequency being 1/3 that of CLK0 (i.e. with a period three times that of CLK0). In summary, if a frequency divider of the present invention is designed to divide an original clock into a target clock with a frequency factor equal to 3, the middle set circuit of the frequency divider has to comprise nothing but only one clock generator, i.e. the second clock generator, without including any first sets of clock generators.

Please refer to Fig.5 and Fig.6. The dividing circuit 104 of the non-integer frequency divider 100 outputs divided clocks with a frequency being 1/5 that of CLK0 from the end A. The middle set circuit 114 of the dividing circuit 104 comprises two serially connected clock generators 152 and 154. In summary, if a frequency divider of the present invention is designed to divide an original clock into a target clock with a frequency factor equal to 5, in addition to the second clock generator, the middle set circuit of the frequency divider has to comprise one first set of clock generator.

Please refer to Fig.8. The four dividing circuits of the frequency divider 801 output divided clocks with a frequency being 1/15 that of CLK0. In addition to the second clock generator, the middle set circuit of each of the dividing circuits comprises six serially connected clock generators.

In summary, if a frequency divider of the present invention

is designed to divide an original clock into a target clock with a frequency factor M being a positive odd number (for example 3, 5 and 15), in addition to the second clock generator, a middle set circuit of the frequency divider has to further comprise **(M-3)/2 ((3-3)/2=0, (5-3)/2=1, (15-3)/2=6) serially connected first sets of clock generators.**

Therefore, M-1 is replaced by (M-3)/2 to fix typos.

Sincerely,

Winston Hsu Date: 9/9/2004

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506
Merrifield, VA 22116
U.S.A.
e-mail : winstonhsu@naipo.com
(Please contact me by e-mail if you need a telephone communication and I will return your call promptly.)